Notice of Allowability	Application No.	Applicant(s)	
	10/016,196	NGO ET AL.	
	Examiner	Art Unit	
	Jason M. Perilla	2638	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed April 20, 2005*.

2. ☒ The allowed claim(s) is/are *claims 1-7, 9-28, 30 and 32 renumbered respectively as claims 1-29*.

3. ☒ The drawings filed on *20 April 2005* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *20050707* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. Claims 1-28 and 30-32 are pending in the instant application.

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Kevin J. Canning (35,470) on July 7, 2005.

The application has been amended as follows:

The following version of claim 1 replaces all prior versions of the claim in their entirety.

1. A system for synchronous communication between a first integrated circuit and a second integrated circuit comprising:

a synchronous interconnect structure for correcting a timing alignment of a data signal and a source clock signal between said first integrated circuit and said second integrated circuit each time said data signal and said source clock signal are transmitted across said synchronous interconnect structure, wherein said synchronous interconnect structure comprises,

a control circuit to control an amount of ~~a~~ propagation delay inserted into a first transmission path and a second transmission path, wherein said data signal propagates on said first transmission path and said source clock signal propagates on said second transmission path; ~~and~~

a phase-locked loop circuit to provide said control circuit with a time varying signal that indicates when the amount of propagation delay inserted into said first and second transmission paths should be inserted,

a detection circuit to determine and assert a correction signal if the amount of propagation delay inserted into said first and said second transmission paths needs adjustment; and

a delay circuit that inserts the amount of propagation delay into said first and said second transmission paths based on said time varying signal provided by said phase-locked loop circuit and said correction signal asserted by said detection circuit, wherein said detection circuit comprises

a phase detector to detect a phase differential between said source clock signal and said data signal following the insertion of the amount of propagation delay into said first and said second transmission paths, and

a counter to track the phase differential determined by said phase detector and assert said correction signal that indicates a direction said timing alignment should shift.

Regarding claim 3, in line 12, "receiver is a part" is replaced by –receivers are a part--.

Claim 8 is CANCELED.

The following versions of claims 9 and 10 replace all prior versions of the claims in their entirety.

9. The system of claim ~~8~~ 1, wherein said detection circuit further comprises:

~~a phase detector to detect a phase differential between said source clock signal and said data signal following the insertion of said propagation delay into said first and said second transmission path;~~

~~a counter to track the phase differential determined by said phase detector and assert said correction signal that indicates a direction said timing alignment should shift; and~~

a fault detector to detect when said data signal and said source clock signal toggle to allow said counter to track said phase differential when said data signal and said source clock signal both toggle.

10. The system of claim ~~8~~ 1, wherein said delay circuit comprises,

a first delay element to insert said amount of propagation delay into said first transmission path ~~within said receiver~~;

a second delay element to insert said amount of propagation delay into said second transmission path ~~within said receiver~~; and

a finite state machine to interpret said correction signal asserted by said counter to control ~~an~~ the amount of ~~said~~ propagation delay inserted into said first and second transmission paths by said delay circuit.

Regarding claim 11, in line 1, "The system of claim 7" is replaced by –The system of claim 1--.

Regarding claim 15, in line 3, "said loop filter" is replaced by –a loop filter--.

Regarding claim 16, in line 2, "printed circuit board. (PCB)." is replaced by –printed circuit board (PCB). --.

Regarding claim 25, in line 2, "element comprise" is replaced by –elements each comprise--.

The following version of claim 28 replaces all prior versions of the claim in their entirety.

28. A deskewing circuit to perform a timing alignment of a synchronous point-to-point signal on a per signal basis comprising,

a control circuit to control said timing alignment of said synchronous point-to-point signal, wherein the control circuit comprises:

a detection circuit detecting a phase differential between a first data signal of said synchronous point-to-point signal and a source clock-signal of said synchronous point-to point signal; ~~and~~

a delay circuit delaying both said first data signal and said source clock-signal based on an output signal of said detection circuit, wherein said detection circuit comprises

a counter circuit to count an occurrence of said phase differential and assert said output signal after a predetermined count; and

a fault detector circuit to detect a false count by said counter circuit, wherein upon detection of said false count said fault detector circuit instructs said counter circuit to disregard said false count.

Claim 31 is CANCELED.

Regarding claim 32, in line 1, "further comprises" is replaced by –further comprising--.

Claims 1-7, 9-28, 30 and 32 are renumbered as claims 1-29 respectively, and the claim dependency is renumbered accordingly.

Allowable Subject Matter

3. Claims 1-7, 9-28, 30 and 32 renumbered respectively as claims 1-29 are allowed.

4. The following is an examiner's statement of reasons for allowance:

Claims 1-7, 9-28, 30 and 32 renumbered respectively as claims 1-29 are allowed because the prior art of record does not anticipate or obviate the claimed subject matter.

Independent claim 1 is allowable over the prior art of record because the prior art of record does not disclose the various components of the claimed system or an obvious combination thereof. Independent claim 18 is allowable over the prior art of record because the prior art of record does not disclose the detection of a first phase offset between a source clock signal and a feedback signal to generate a time varying signal and the detection of a second phase offset between the source clock signal and a data signal to generate delay values wherein the source clock signal and the data signal are time adjusted according to the time varying signal and the delay values. Independent claim 28 is allowable over the prior art of record because the prior art of record does not disclose the counting of a phase differential between a source clock signal and a data signal and a fault detector which inhibits the count of the phase differential upon the detection of a false count.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following prior art of record is cited to show the current state of the art with respect to data and clock synchronoizers.

U.S. Pat. No. 4965814 to Yoshida et al.

U.S. Pat. No. 6539072 to Donnelly et al.

U.S. Pub. No. 2002/0006177 to Pickering et al.

U.S. Pat. No. 6836503 to Best et al.

U.S. Pat. No. 6570944 to Best et al.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason M. Perilla whose telephone number is (571) 272-3055. The examiner can normally be reached on M-F 8-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vanderpuye Kenneth can be reached on (571) 272-3078. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason M. Perilla
July 7, 2005

jmp

CHIEH M. FAN
PRIMARY EXAMINER